REMARKS

Claims 1 and 4 are amended. No new subject matter is added. Reconsideration and allowance of claims 1-20 is requested in light of the following remarks.

Claim Rejections - 35 USC § 102

Claims 1 and 3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,245,669 to Fu, et al. ("Fu"). The applicant disagrees.

Claim 1 recites depositing a multi-layered hard mask layer on the wire line layer, the multi-layered hard mask layer including at least a first hard mask layer, a second hard mask layer, and a third hard mask layer, each of the first, second, and third hard mask layers formed of different insulating materials to have an etch selectivity with respect to each other. Claim also recites patterning the multi-layered hard mask layer using a photoresist pattern to produce a multi-layered hard mask. This last feature is fully supported by the original application at, e.g., page 6, lines 15-20.

It is alleged that Fu discloses a wire line layer (14, FIG. 4), a first hard mask (16; FIG. 4), a second hard mask (18; FIG. 4), and a third hard mask (21; FIG. 4).

To the contrary, Fu's layer 21 is not a hard mask at all but a ***photoresist layer 21*** that is used to pattern the hard mask layer 16, 18 (column 10, lines 22-23; emphasis added). Since it is apparent that Fu's multi-layered hard mask layer consists only of layer 16 and layer 18, Fu fails to teach the recited third hard mask layer.

Furthermore, claim 1 recites patterning the wire line layer using the multi-layered hard mask to form wire lines. The multi-layered hard mask was previously defined to include first, second, and third hard masks. Thus, the third hard mask of the multi-layered hard mask is used as an etch mask in patterning the wire line layer to form wire lines.

It was stated in the Advisory Action that "[t]he three hardmasks are present under the resist at this time, therefore they are part of the patterning process." To the contrary, Fu teaches that the alleged wire line layer (polysilicon layer 14) is not etched to form gate electrodes 14 until after the alleged third hard mask (photoresist layer 21) has been removed (column 10, line 29-32). Consequently, it cannot be said that all three of Fu's hardmasks (16/18/21) are present at the time when the alleged wire line layer (polysilicon layer 14) is patterned.

Thus, Fu does not pattern the alleged wire line layer using the alleged multi-layered hard mask 16/18/21, but rather a multi-layered hard mask that consists only of layers 16 and 18.

Additionally, claim 1 recites forming interconnecting contacts that align with the wire lines and vertically penetrate the insulating layer where the first hard mask is protected by the second hard mask.

Remembering that the recited wire line layer is allegedly taught by Fu's gate electrode 14, it is also alleged that the recited insulating layer is taught by Fu's ILD layer 30 (FIG. 8). Although it is not stated, the recited interconnecting contacts are apparently alleged to be taught by Fu's first opening 42 (FIG. 1) or Fu's contact opening 43 (FIG. 8).

FIGs. 1-3 of Fu fail to show any alignment between the alleged interconnecting contacts 42 and the alleged wire line layer 14. While FIG. 8 of Fu does show a relationship between the alleged interconnecting contact 43 and the alleged wire line layer 14, the contact 43 cannot be said to be "aligned" with the wire line layer 14 as recited in the claim.

"Aligned" is a feature that is explicitly recited in claim 1. Although pending claims are given the broadest reasonable interpretation, this interpretation is limited in that it must be consistent with the specification. MPEP 2111. Reading the claims in light of the specification to interpret a feature that has an express basis in the claim is allowed. MPEP 2111. The specification teaches that the bit line contacts 410, which are interconnecting contacts, are used to electrically connect the active region 110 of the semiconductor substrate with the bit lines through the first contact pads 310 (page 5, lines 13-15). Thus, at the very least, "aligned" should be interpreted to mean that the interconnecting contacts electrically connect the active region to the bit lines (the recited wire line layer).

Contrary to this feature, Fu FIG. 8 shows that the alleged interconnecting contact 43 does not electrically connect the alleged wire line layer 14 to the active region.

Also contrary to claim 1, Fu FIGs. 1-8 fail to show that the alleged interconnecting contacts 42 or 43 vertically penetrate the alleged insulating layer 30 in a region where the alleged first hard mask 16 is protected by the alleged second hard mask 18.

For any of the reasons given above, Fu does not anticipate claim 1 because it fails to show the identical invention in as complete detail as is contained in the claim. MPEP 2131.

Claim 3 depends from claim 1 and inherently contains the features of claim 1. Consequently, Fu fails to anticipate claim 3 for at least the same reason that is fails to anticipate claim 1.

Claim 4 recites forming a multi-layered hard mask, the multi-layered hard mask including a first hard mask, a second hard mask, and a third hard mask. Claim 4 also recites patterning the wire line layer using the multi-layered hard mask, as well as forming openings to be aligned with the wire lines and that vertically penetrate the insulating layer where the first hard mask disposed on the wire lines is protected by the second hard mask. All of these recited features are similar to the features of claim 1 that were discussed above.

Thus, for any of the reasons given for claim 1, Fu also fails to anticipate claim 4 because it does not show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Additionally, claim 4 is amended to recite forming interconnecting contacts that electrically connect the wire line layer to an active region of a semiconductor substrate by filling the openings and by node-separating the conductive layer. This feature is fully supported by the original application at, e.g., claim 4 and page 5, lines 13-15.

Fu makes no mention that electrical interconnects are formed by node-separating the alleged conductive layer 30 (column 8, lines 35-40).

Fu FIG. 8 also shows that shows that the alleged interconnecting contact 43 does not electrically connect the alleged wire line layer 14 to the active region.

For these two additional reasons, Fu also fails to anticipate claim 4 because it does not show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claim 5 depends from claim 4 and inherently contains the features of claim 4. Consequently, Fu fails to anticipate claim 5 for at least the same reasons that is fails to anticipate claim 4.

Claims 1 and 3-4 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,534,389 to Ference, et al. ("Ference"). The applicant disagrees.

Claim 1 recites depositing a multi-layered hard mask layer on the wire line layer, the multi-layered hard mask layer including a first hard mask layer, a second hard mask layer, and a third hard mask layer. Claim 1 further recites patterning the multi-layered hard mask layer using a photoresist pattern to produce a multi-layered hard mask, and patterning the wire line layer using the multi-layered hard mask.

It is alleged that Ference discloses a wire line layer (conductive polysilicon layer 14; FIG. 1) as well as a first hard mask layer (first TEOS layer 16; FIG. 1; column 4, lines 35-36) a second hard mask layer (silicon nitride layer 18; FIG. 1; column 4, line 36), and a third hard mask layer (second TEOS layer 20; FIG. 1; column 4, line 37).

However, Ference discloses that a "polysilicon conductor (PC) photoresist mask (***not shown***) is used when the alleged wire line layer 14 is etched to form gate stacks 22, 24 (FIG. 3; column 4, lines 54-56; emphasis added).

Thus, Ference does not teach patterning the alleged wire line layer 14 using the alleged multi-layered hard mask 16, 18, 20. Rather, Ference teaches that the alleged wire line layer 14 is patterned with a PC photoresist mask.

Furthermore, claim 1 recites that each of the first, second, and third hard mask layers are formed of a different insulating material. To the contrary, Ference's alleged first hard mask (first TEOS layer 16) and the alleged third hard mask (second TEOS layer 20) are formed of the same (TEOS) material, as was indicated above.

Furthermore, claim 1 recites forming interconnecting contacts that are aligned with the wire lines and vertically penetrate the insulating layer where the first hard mask is protected by the second hard mask.

To date, it is alleged simply that "[c]ontacts to memory devices are discussed." "Aligned" is a feature that is explicitly recited in claim 1. Although pending claims are given the broadest reasonable interpretation, this interpretation is limited in that it must be consistent with the specification. MPEP 2111. Reading the claims in light of the specification to interpret a feature that has an express basis in the claim is allowed. MPEP 2111. The applicant's specification at, e.g., FIGs. 8 and 9, illustrate that the bit line stacks 500 are centered over the bit line contacts 410.

However, Ference FIG. 7 illustrates that the interconnecting contacts are not aligned with the wire lines in a manner that is consistent with the applicant's specification.

Additionally, contrary to claim 1, Ference FIG. 7 illustrates that the alleged interconnecting contacts do not vertically penetrate the alleged insulating layer 54 where the alleged first hard mask 16 is protected by the alleged second hard mask 18.

For any of the above reasons, Ference fails to anticipate claim 1 because it does not teach the identical invention in as complete detail as is contained in the claim. MPEP 2131.

Claim 3 depends from claim 1 and inherently contains the features of claim 1. Consequently, Ference fails to anticipate claim 3 for at least the same reason that is fails to anticipate claim 1.

Claim 4 recites forming a multi-layered hard mask, the multi-layered hard mask including a first hard mask, a second hard mask, and a third hard mask. Claim 4 also recites forming wire lines by patterning the wire line layer using the multi-layered hard mask, as well as forming openings to be aligned with the bit lines and vertically penetrate the second

insulating layer and the first insulating layer where the first hard mask disposed on the bit lines is protected by the second hard mask.

The above features of claim 4 are similar to the features found in claim 1 that were discussed above. Thus, for any of the reasons given for claim 1, Ference also fails to anticipate claim 4 because it does not show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claim Rejections - 35 USC § 103

Claims 2 and 6-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ference. The applicant disagrees.

Claim 2 depends from claim 1, and inherently contains the features of claim 1. It was demonstrated above that Ference fails to teach all the features of claim 1. Consequently, claim 2 is allowable at least because any claim that depends from a nonobvious independent claim is also allowable. MPEP 2143.03.

With regard to claim 6, it is apparently alleged that Ference discloses the feature of forming a bit line layer (conductive polysilicon layer 14; FIG. 1) on a first insulating layer (unspecified).

It is apparently alleged that Ference discloses the feature of forming a multi-layered hard mask on the bit line layer 14, the multi-layered hard mask including a first hard mask (first TEOS layer 16; FIG. 1; column 4, lines 35-36), a second hard mask (silicon nitride layer 18; FIG. 1; column 4, line 36), and a third hard mask (second TEOS layer 20; FIG. 1; column 4, line 37).

However, contrary to claim 6, the first, second, and third hard masks are not each formed of a different material, as evidenced by the fact that the alleged first and third hard masks are both composed of TEOS.

It is apparently alleged that Ference discloses the feature of patterning the bit line layer 14 using the third hard mask 20 as an etch mask to form bit lines.

To the contrary, Ference actually teaches that a "polysilicon conductor (PC) photoresist mask (***not shown***) is used when the alleged bit line layer 14 is etched to form gate stacks 22, 24 (FIG. 3; column 4, lines 54-56; emphasis added).

It is apparently alleged that Ference discloses the feature of forming a second insulating layer (insulative material 54; FIG. 6; column 5, line 41) on the third hard mask 20 to fill gaps between the bit lines 14.

To the contrary, Ference actually teaches that the alleged second insulating layer 54 is formed on a nitride barrier 36 (FIG. 6; column 5, line 46). The alleged third hard mask 20 is not even present at this stage (FIG. 6).

It is apparently alleged that Ference discloses the feature of forming openings (unspecified) to be aligned with the bit lines 14 and vertically penetrate the second insulating layer 54 and the first insulating layer (unspecified) where the first hard mask 16 disposed on the bit lines is protected by the second hard mask 18.

To the contrary, assuming that Ference's electrically insulative dielectric layer 13 (FIG. 1; column 4, lines 29-30) corresponds to the recited first insulating layer, Ference FIGs. 6 and 7 illustrate that the openings do not vertically penetrate the first insulating layer where the first hard mask 16 disposed on the bit lines 14 is protected by the second hard mask 18.

It is apparently alleged that Ference discloses the feature of forming insulating spacers (sidewall spacers 26/42/36/46 on the sidewalls of the openings (unspecified).

To the contrary, assuming that Ference's openings correspond either to cavity 38 that is filled with source/drain contact 34 (FIG. 6; column 5, lines 54), or to cavity 66 that is filled with the single level contact 70 (FIG. 7; column 6, lines 18-23), Ference FIG. 7 shows that no spacer is formed on sidewalls of the openings. Spacer 44 existed prior to formation of the cavity 38 (see, e.g., FIGs. 4B, 6, and 7). There are no insulating spacers formed on the sidewall of cavity 66 (see, e.g., FIG. 7).

For any of the reasons stated above, Ference fails to establish a *prima facie* case of obviousness for claim 6 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 7-20 depend from claim 6, and inherently contain the features of claim 6. For any of the reasons stated above, claim 6 is nonobvious with respect to the Ference reference and consequently, claims 7-20 are allowable at least because any claim that depends from a nonobvious independent claim is also allowable. MPEP 2143.03.

Conclusion

For the above reasons, reconsideration and allowance of claims 1-20 is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Todd J. Iverson
Reg. No. 53,057

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613
Customer No. 20575

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on October 20, 2005.

Stormi R. Davis